

Company profile

Jan-2016



1. Company Profile

2. TECNISCO Products

- for MEMS
- for Life Science
- for High Power Laser Heat Sink

Head office: Tokyo / Japan

Factory: (1)Kure, Hiroshima / Japan
(2)Suzhou / China

Incorporated: Feb. 1970

Employees: 298 (Mar. 2015)

TECNISCO JAPAN 137
TECNISCO Suzhou 161

Certification : ISO9001, ISO14001
ISO/TS16949





- Dicing
- Ultrasonic machining
- Sandblasting
- Milling (Drilling) /CNC machining
- Assembling (Solder: AuSn, AuGe, AgCuIn, AgCu) Eutectic solder
280°C, 380°C, 650°C, 800°C
- Polishing
- Bonding (Glass-Glass: Diffusion, Glass-Si: Anodic)
- Sputtering (Cr, Ti, Pt, Au, Ni.)
- Vapor deposition (AuSn, AuGe)
- Plating (Ni, Au,Cu etc.)
- Etching

ALL IN ONE
Easy to control quality and lead time

- Metals
 - Cu, Fe, Ag, Mo, Ni
 - CuW (Cu ration : 10, 15, 20 wt%)
 - Kovar (Fe-Ni-Co)
 - SUS (Stainless steel)
 - Fe-Ni Alloy
 - Cu-Mo-Cu *
 - Cu-AlN-Cu *
- *Electroformed material for CTE match
- Ceramics
 - AlN (170W, 200W, 230W)
 - Al₂O₃

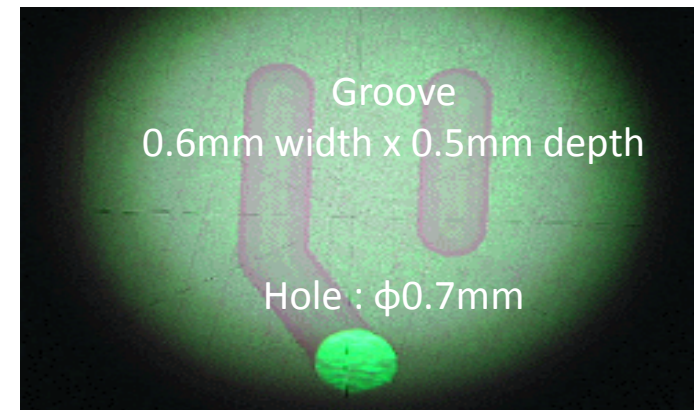
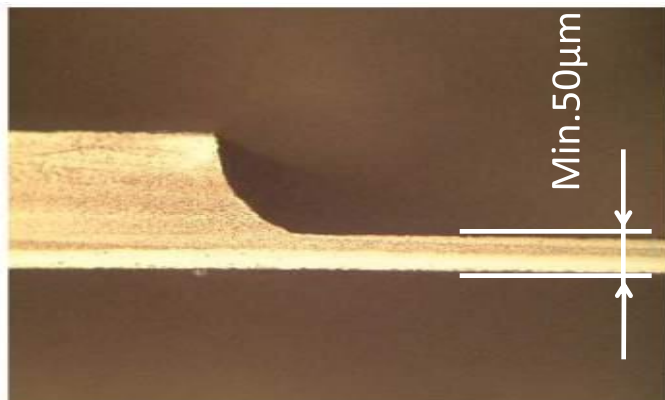
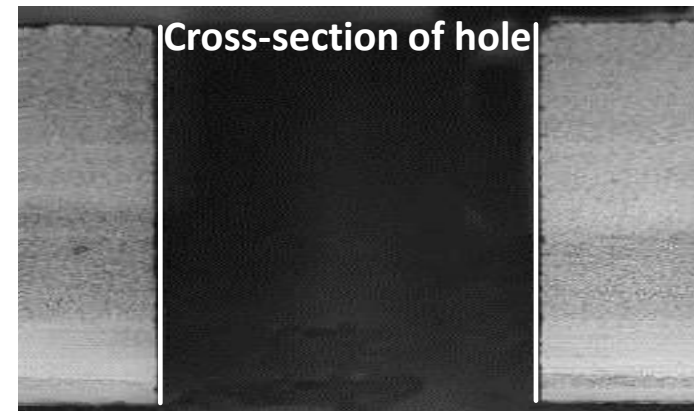
- Glass line
 - Borofloat 33, D263T, AF45 (SCHOTT)
 - Eagle XG eco, 0211 (Corning)
 - SD2 (HOYA)
 - SW-YY (AGC)
 - BK7

- Quartz

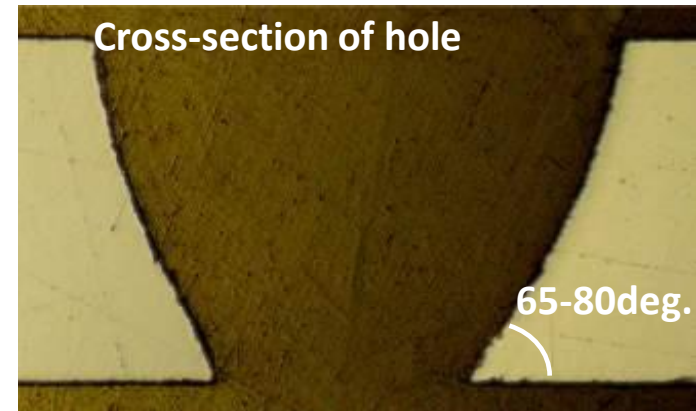
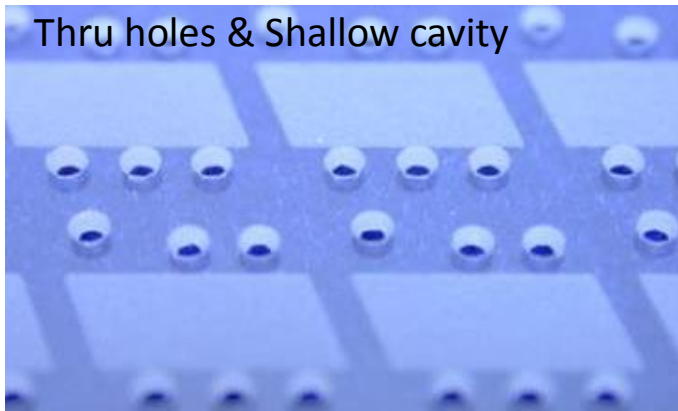
- Si

Wafer size 1 to 8inch
(Round and square)

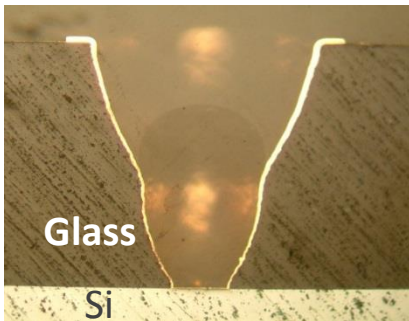
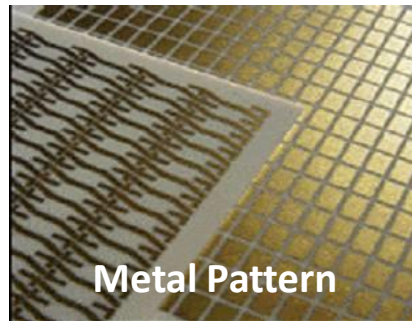
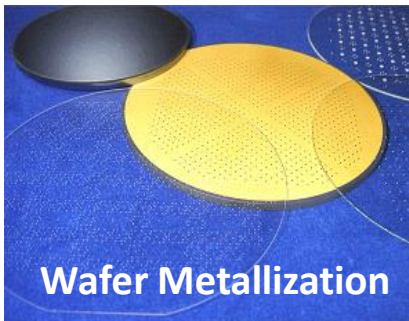
- CNC machining/drilling process
- Vertical straight thru holes
- Thin Cavity. Thru hole on cavity



- Photolithography Process
- Tapered holes (with angle 65-80 deg.)



- Metallization on Glass, Metal, Ceramic, Si, etc...
- Plating / Sputtering/ Vapor deposition
- Ti, Cr, Pt, Au, AuSn, Cu, Ni, etc...
- Electrode by thin film VIA

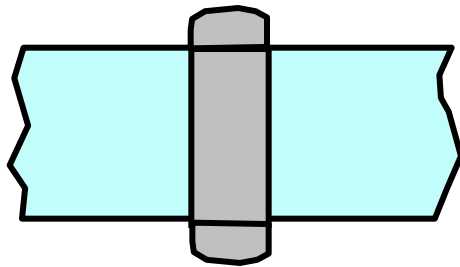


- VIA Height Control

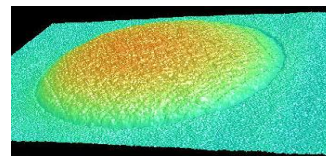
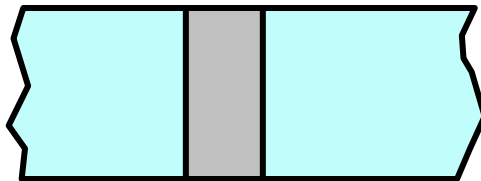
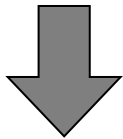
Normal polishing process Via height: $< 4\mu\text{m}$

Original polishing process Via height: $< 1.0\mu\text{m}$

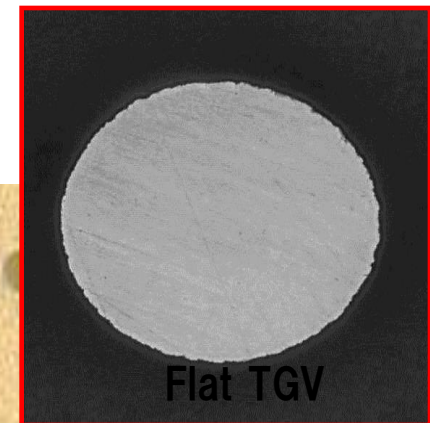
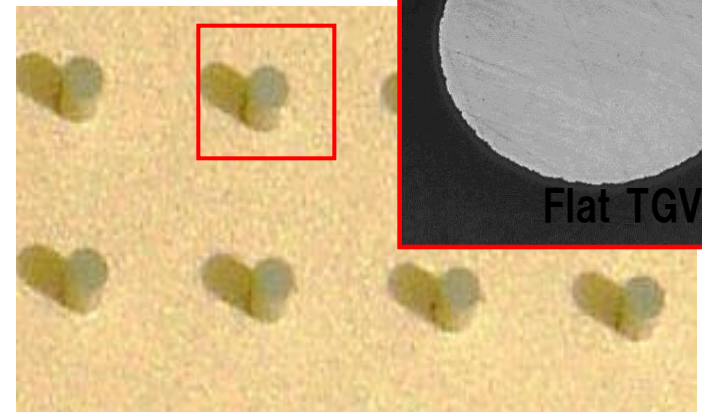
Measurement by interferometer



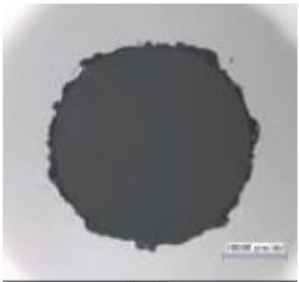

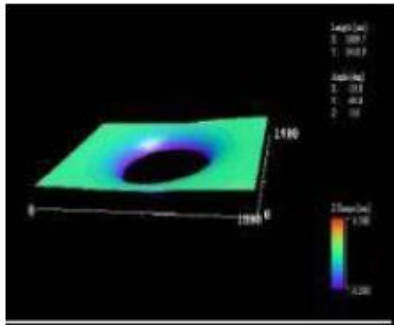

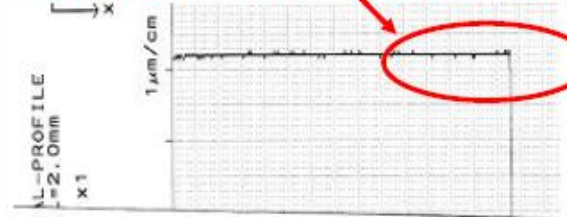
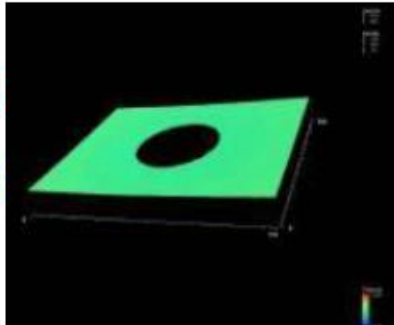
Via Height : $3.4\mu\text{m}$



Via Height : $0.85\mu\text{m}$

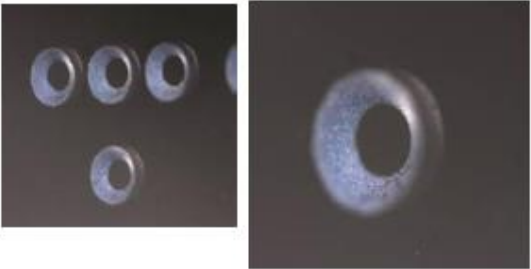




- Advanced Polishing Capability for better bonding performance.
- Designed for Anodic bonding.

	Chipouts	Hole edge quality
Std. polishing	 <p>< 20um</p>	<p>Large slope (400um level) : Non-attach area</p>  
Advanced polishing	 <p>< 5um typ</p>	<p>Sharp edge : Suitable for Anodic bonding</p>  

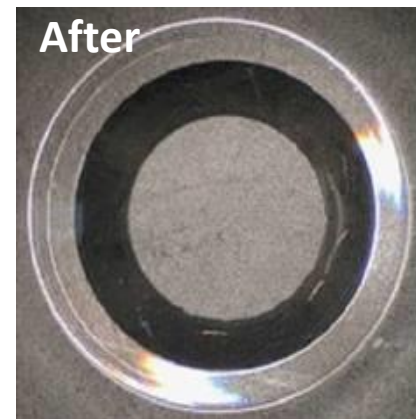
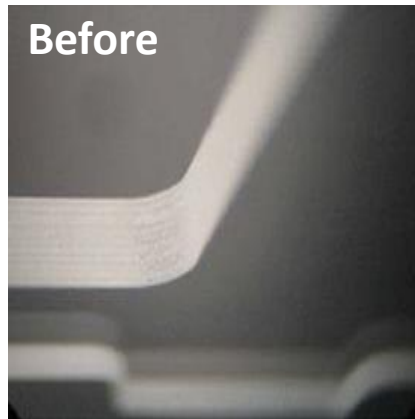
- Micro crack treatment for machined wafers works:
 - => Minimize particles quantity
 - => Prevent the MEMS device error

Comparison of condition (Particle count : >1um / wafer)

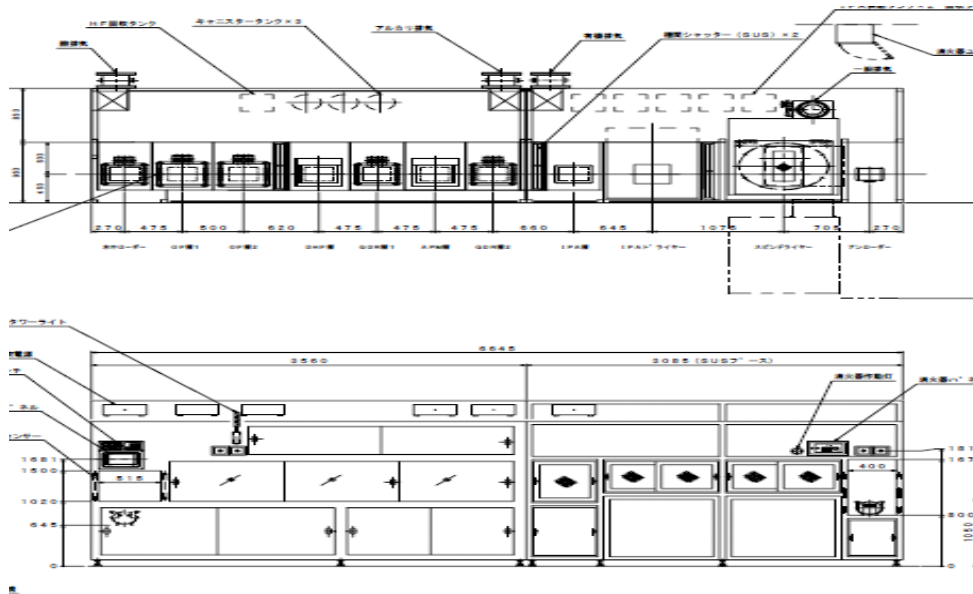
Standard	2 nd grade	1 st grade
		
1,365pcs/wafer	42pcs/wafer	13pcs/wafer

*Particle is measured with 6inch wafer with 4000 holes

- Particle Control
- Surface Treatment

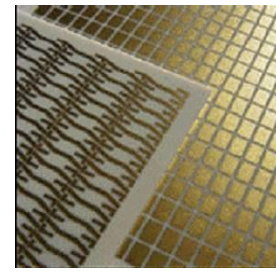
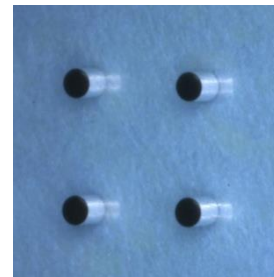
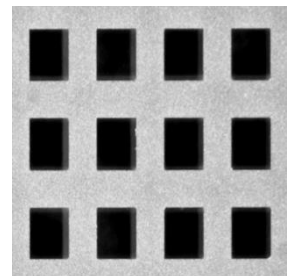
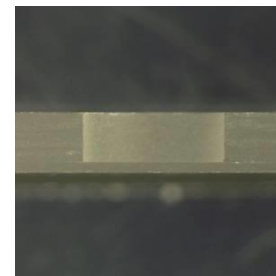
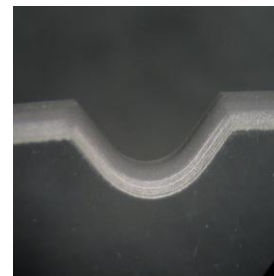
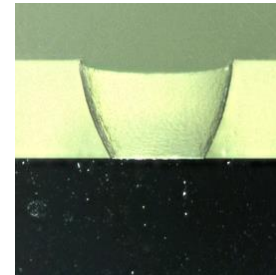
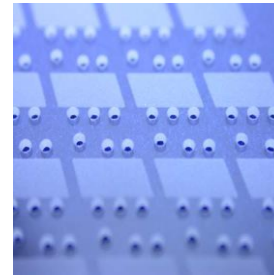
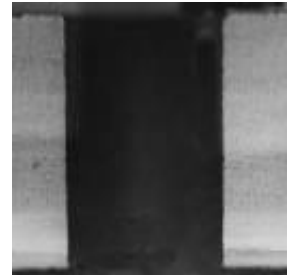
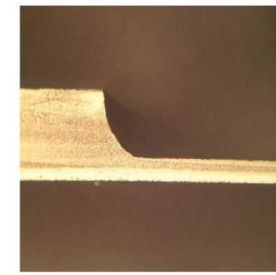
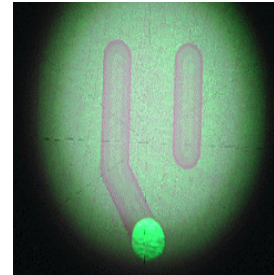


- Fully automatic wafer cleaning machine is installed in clean room class 1000

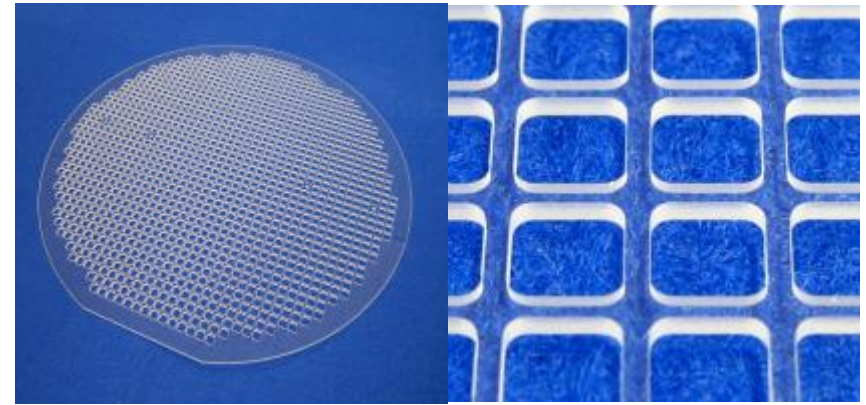
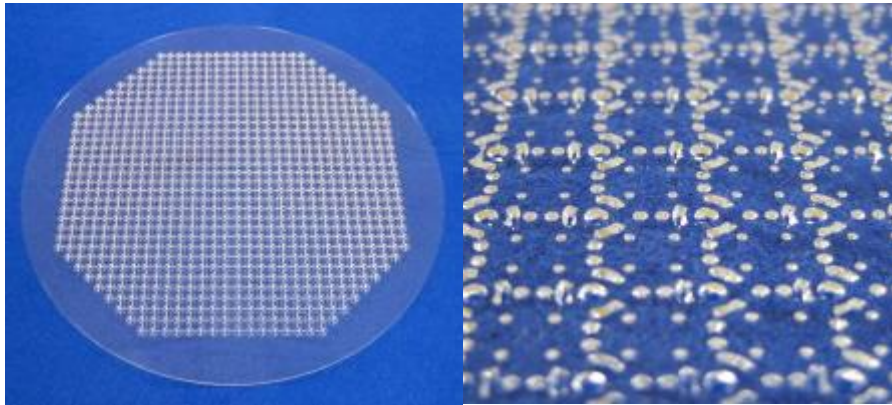


Packing area: Class100

- CNC machining (Drilling)
 - Hole angle is adjustable. (Upto 90 deg.)
- Sandblasting (Powder blasting)
 - Lithographic technology
 - Taper hole(65-80 deg. or more)
- Metallization on glass
 - Lithographic technology
 - Sputtering, Vapor deposition
- Original process:
 - Transparent cavity wafer
 - Mesh/filter glass (Hole size: $\square 0.07\text{mm}$)
 - Through glass via wafer (TGV)
- General process capability:
 - Hole size $\pm 0.02\text{mm}$
 - Hole to hole pitch $\pm 0.02\text{mm}$



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 - **for High Power Laser Heat Sink**

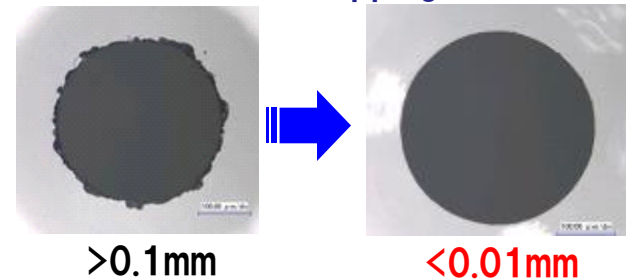


Application

- Sensors (Acceleration, Pressure, Gyro)
- Biomedical chips
- Microreactor etc.

- Minimum hole size : 0.05 mm
- High aspect ratio : up to 1:10
- Wafer size : up to $\phi 200$ mm

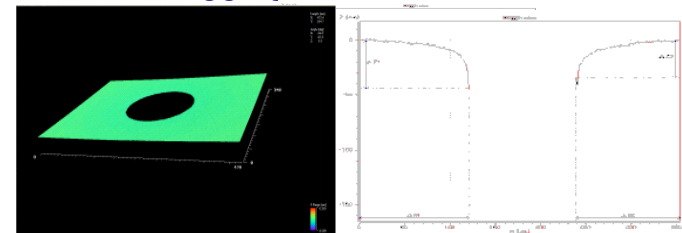
Minimum Chipping



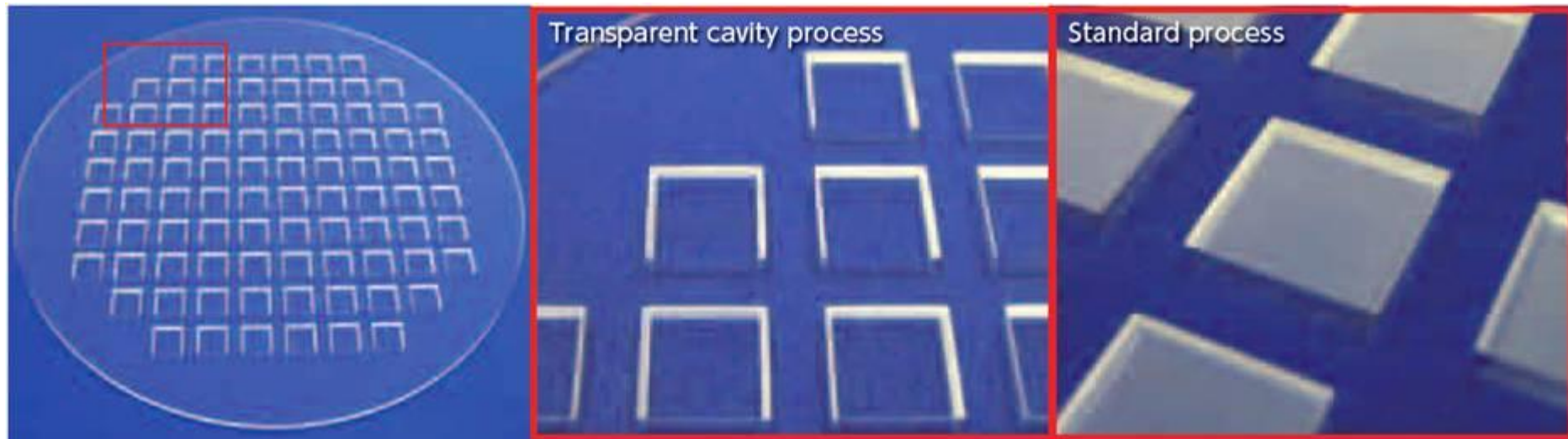
>0.1mm

<0.01mm

Sagging Control



Width < 10 μ m
Depth < 0.1 μ m



Transparent cavity can be used for wide range of wavelength

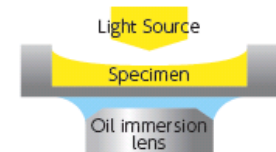
- Sidewall metallization
 - Protect light interference / absorption between holes
- Flexible designing for customer's requirement
- Wafer size up to $\phi 200$ mm
- Focal length of oil immersion lens match with 0.10-0.15mm glass thickness

Application

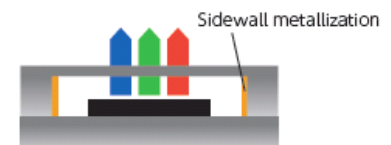
CMOS image sensor cap

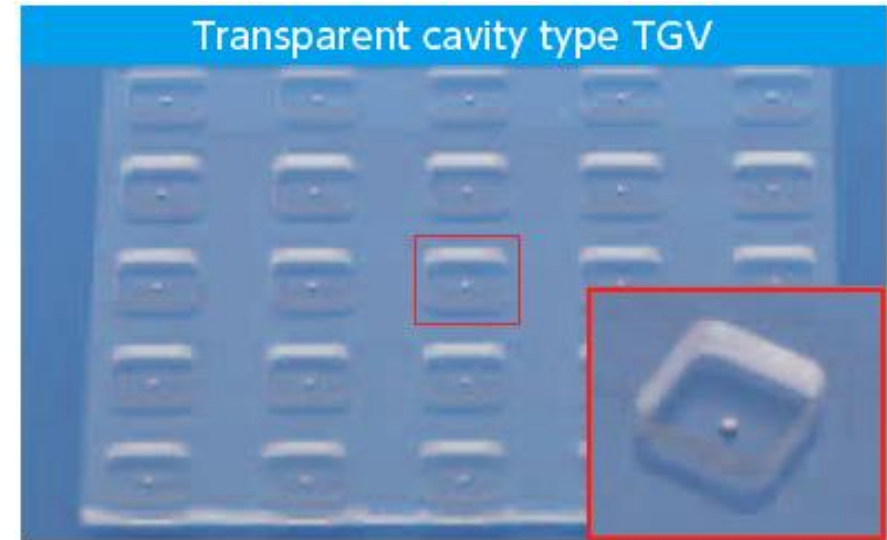
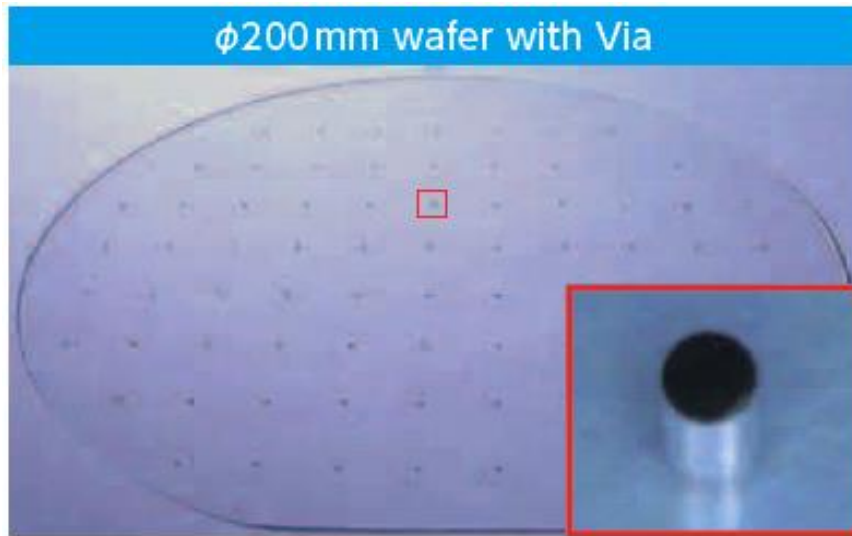


Analytical chip



LD / LED cap

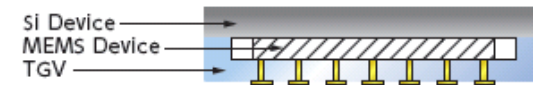




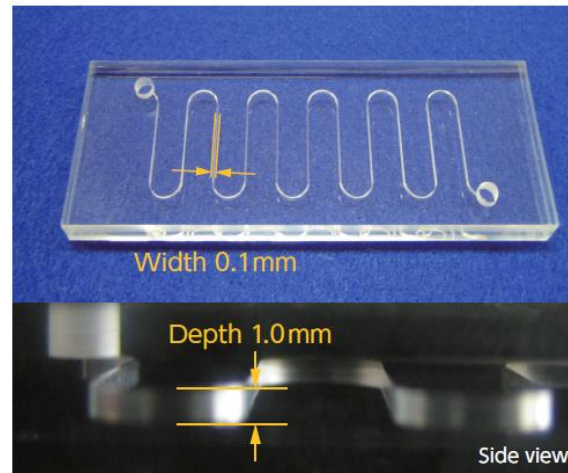
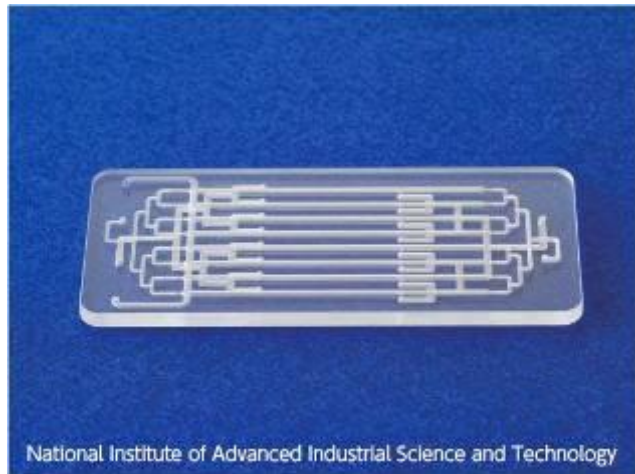
Through Glass Via makes it possible to minimize device

- Anodic bonding process with Si wafer is available
Non glue process is suitable for solving out-gas issue
- Excellence for RF single application
 - Low stray capacitance vs.TSV
 - Low stray inductance
 - Low electric-resistance (Metal-Rod)

TGV application sample



Data	
Via-Glass gap	<1.0 μ m
Permissible temperature	-50℃~450℃
Hermetic level (Helium leakage test)	1×10 ⁻⁹ Pa·m ³ /s



Application

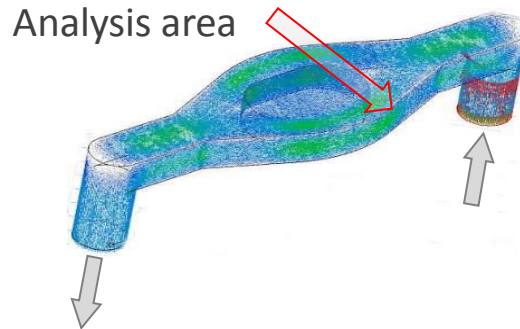
Analytical chips for

- Biomedical
- Medical
- DNA etc.

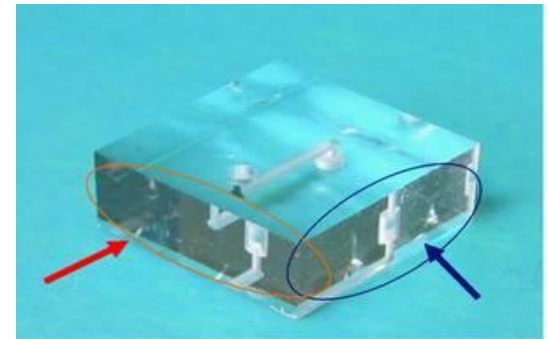
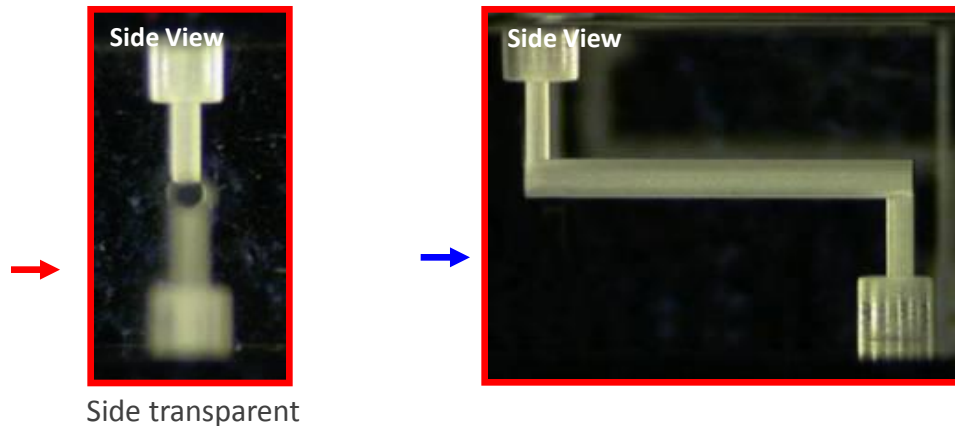
Flexible 3D channel designing up on customer's requirement

- Microfluidic glass chips
 - Excellent for thermal resistance and chemical resistance
- Achieve transparent microfluidic
 - Possible to observe/measure from all direction
- Electrophoresis integration is available for microfluidic
 - Analyte reaction / separation by electrophoresis

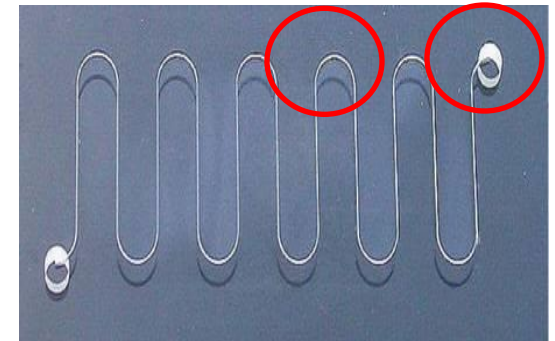
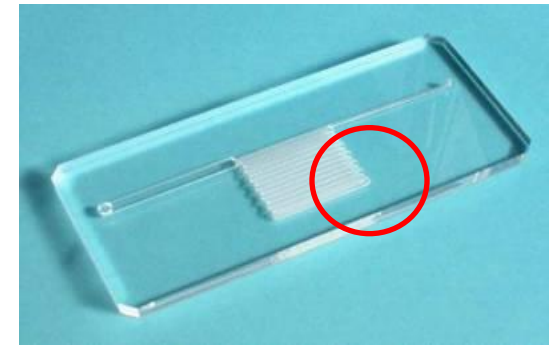
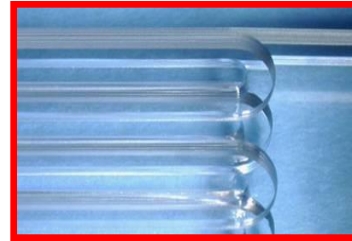
- Microfluidic 1 [with shallow Analysis area]



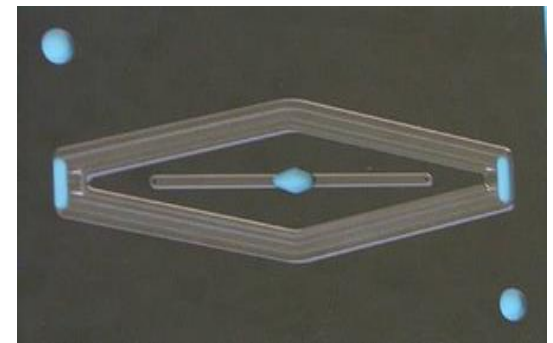
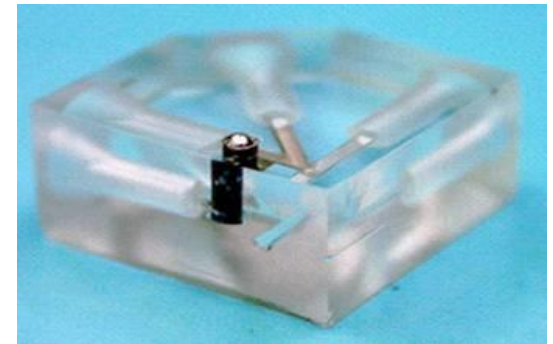
- Microfluidic 2 [with Side Transparent]



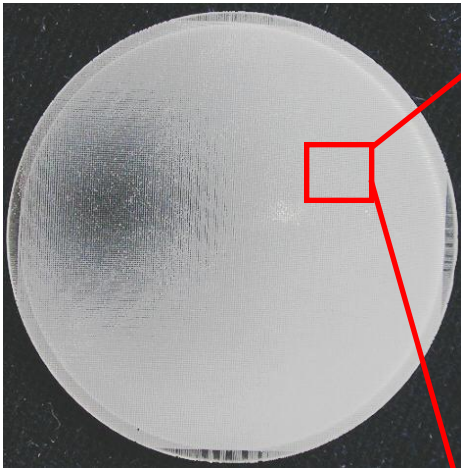
- Microfluidic 3 [with High Aspect Ratio]



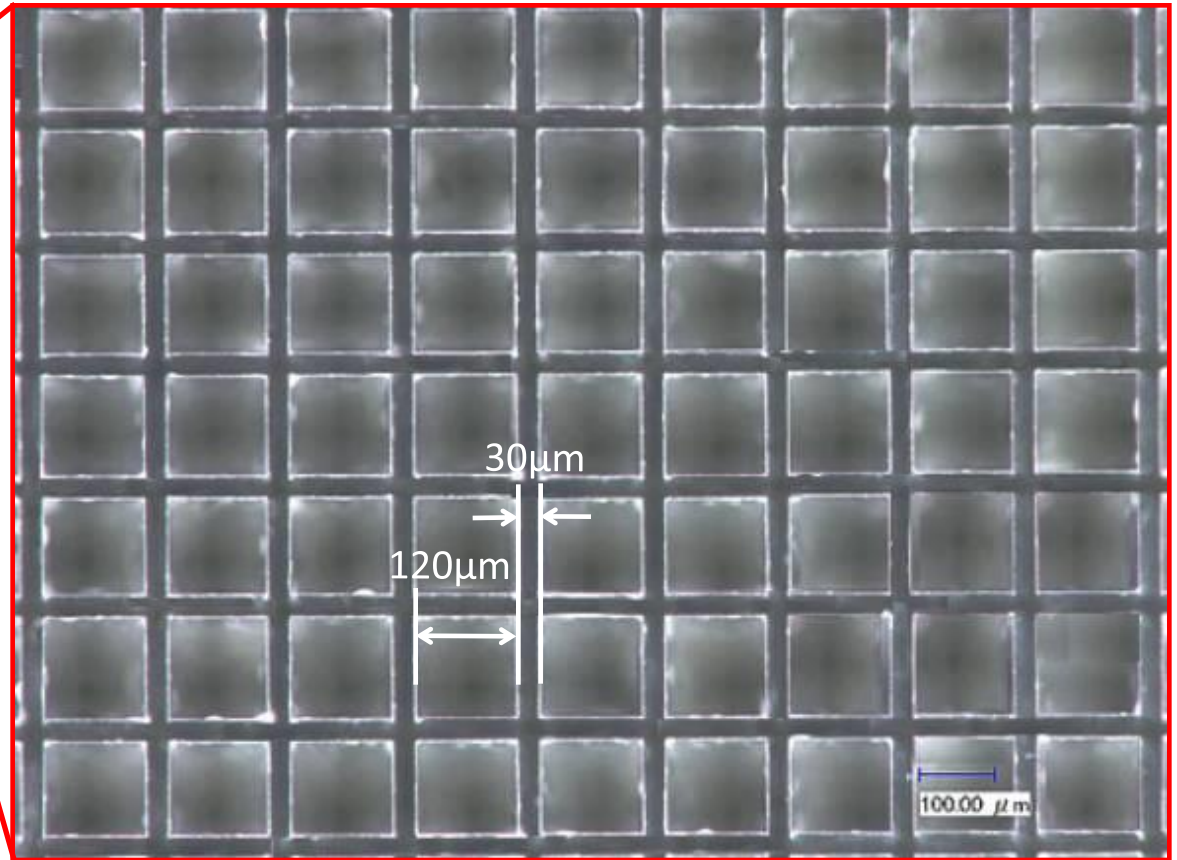
- Microfluidic 4 [with VIA contact]
- Microfluidic 5 [with Tapered Channel]
- Microfluidic 6 [with Isolated Channels]

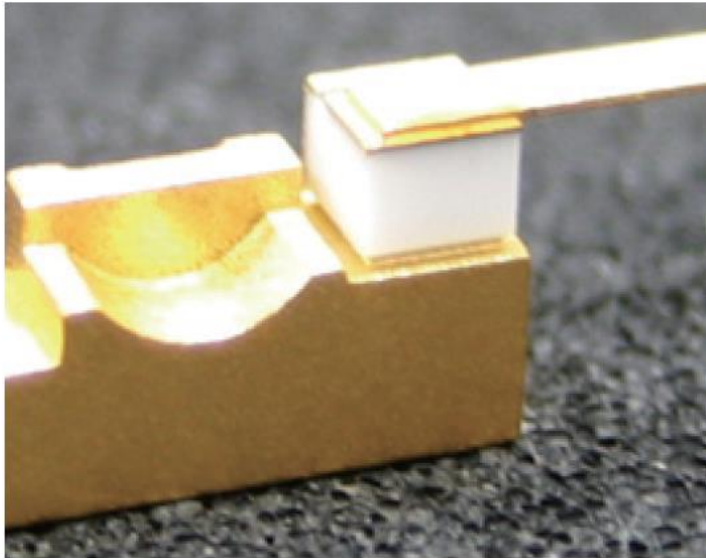


- Numerous holes on glass.



Material: Boroflat33
Wafer size : $\phi 150\text{mm}$
Wafer thickness : 1mm
Hole size : $\square 120\mu\text{m}$
Sash width : $30\mu\text{m}$
Hole pitch : $150\mu\text{m}$



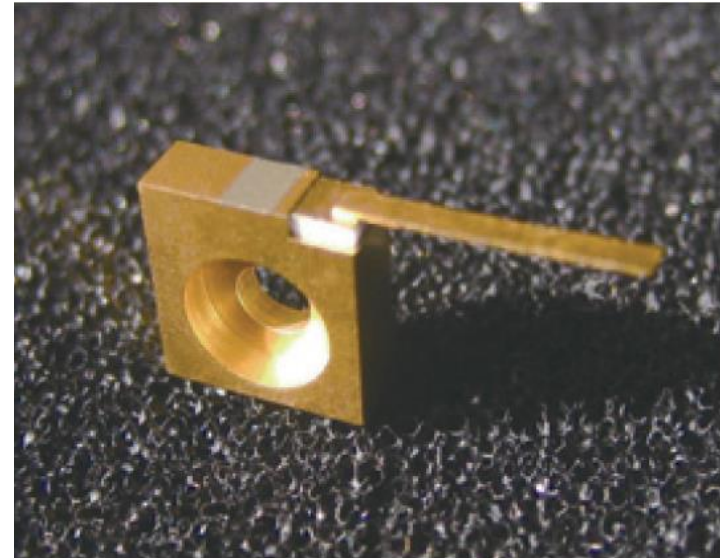


■ Materials

Body	Cu (OFHC) / CuW10
Lead	Kv, Cu, Mo
Ceramic	Al ₂ O ₃ (92-96%)

■ Dimension/Tolerance

Dimension	upon request (Refer image from A to L)
Surface roughness	Ra < 0.4
Edge Radius	≤ 10/50/80 μm



■ Metallization

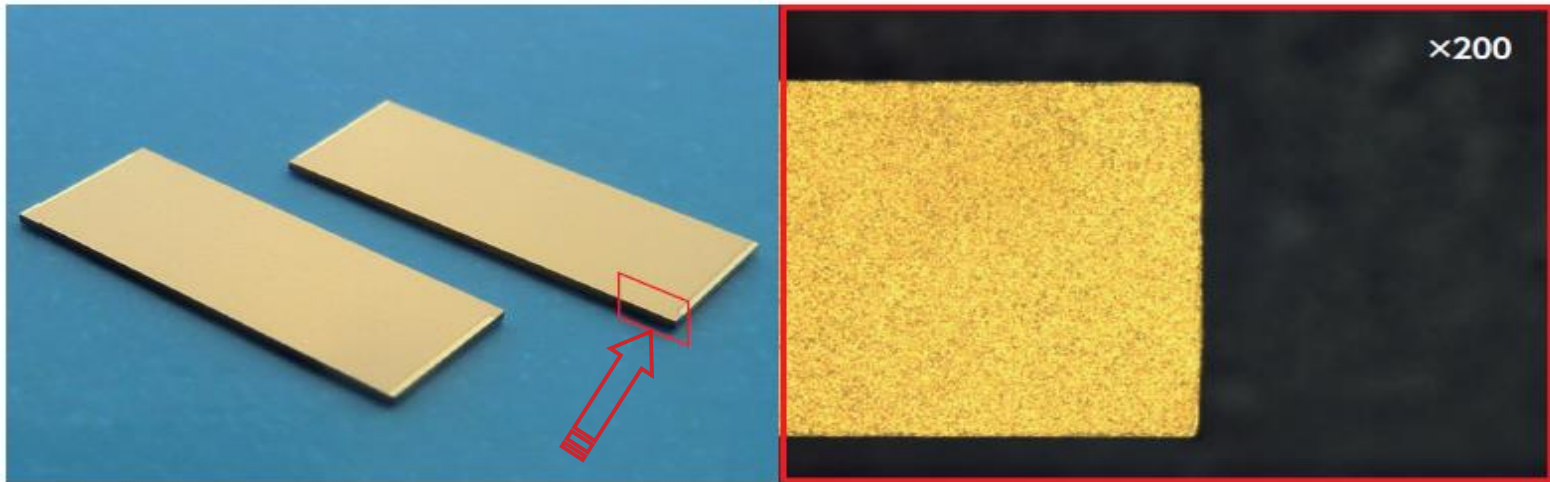
All surface	Ni 1.0-5.0 μm / Au 0.1-0.3 μm
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■ Options

AuSn solder
Diamond turning finish (Top and Front surface)

Applications

- Carrier for opt-telecommunication LD, PD
- Carrier for high power LD



■ Materials

Composition	W90/Cu10
Thermal conductivity	170W/m·K
CTE	6.5ppm/°C

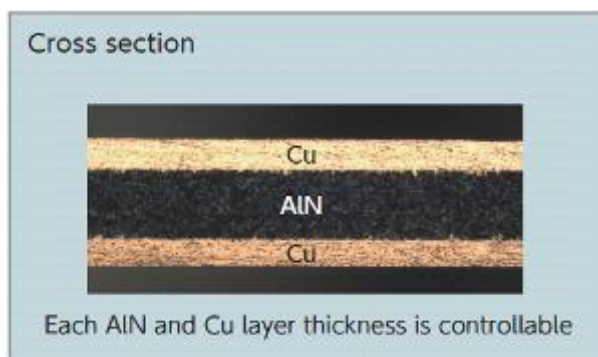
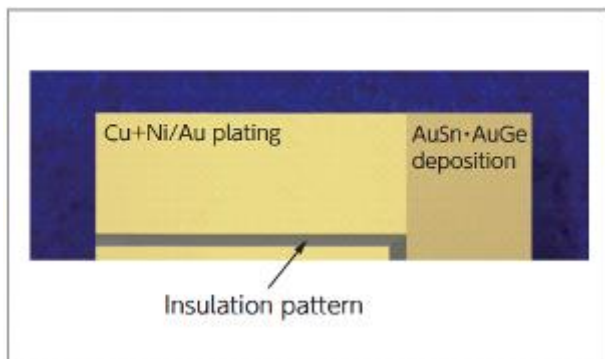
■ Dimension / tolerance

Thickness:	$\pm 20\mu\text{m}$, Length and width: $\pm 50\mu\text{m}$
Surface roughness	$R_a < 0.4$
Warpage	$< 5\mu\text{m}$
Edge Radius	$< 20\mu\text{m}$

■ Metallization

Ni	1-5 μm /Au 0.1-0.3 μm
Au75/Sn25(wt%)	5.0 $\mu\text{m} \pm 1.0\mu\text{m}$

*Sputtering process such as Ti, Pt, Au is also available.



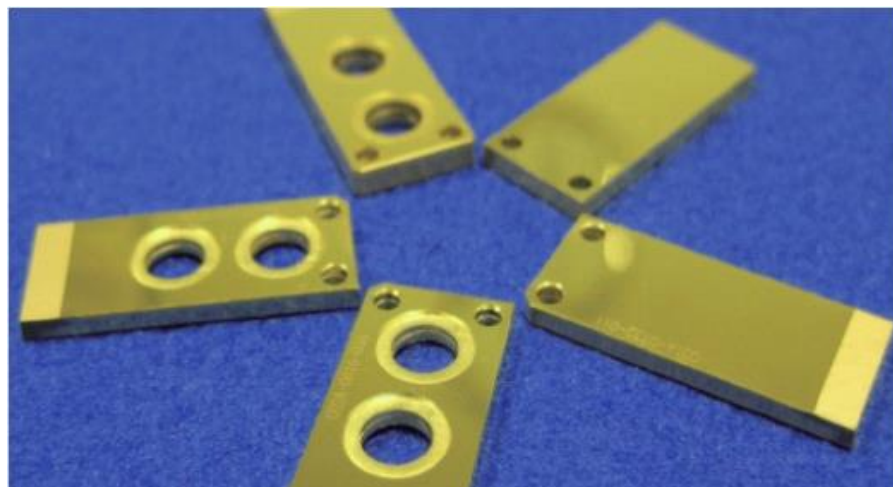
- AlN/Cu composite material contribute to achieve higher thermal conductivity
- Insulation type
- CTE matching with LD
 - Adjusting Cu and AlN thickness makes it possible to control CTE
- Low thermal stress to LD
 - Higher power and longer life
 - Enhance production yield
- AuSn·AuGe solder vapor deposition

Application

- Submount for high power laser diode
- Base for power device

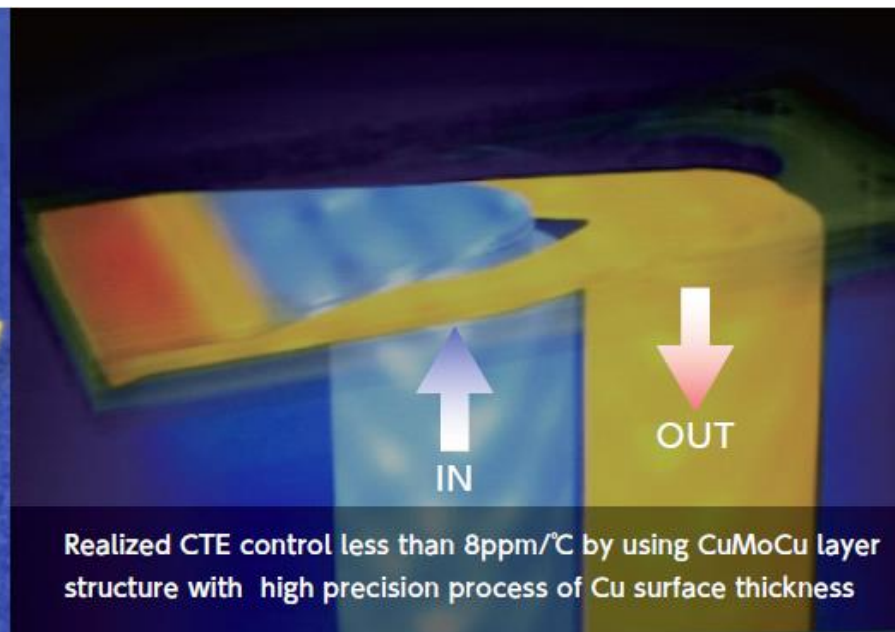
Characteristics comparison data <Reference>

	Unit	Cu-AlN-Cu	AlN	CuW (10/20)
Material features	—	Insulation	Insulation	Conductive
Thermal conductivity	W/m·K	190~250※	170	180 / 200
CTE	ppm/°C	6~10※	4.6	6.5 / 8.3
Electric-resistance	$\Omega \cdot m$	-	-	$5.3 / 4.0 (\times 10^{-8})$
Work voltage	V	<200	<200	NA
Relative permittivity (@1MHz)	-	9	9	NA
Dissipation factor (Tan δ)	-	5×10^{-4}	5×10^{-4}	NA



Application

- Water cooling heatsink for high power LD

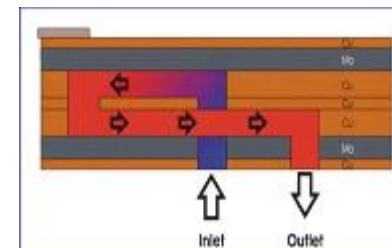
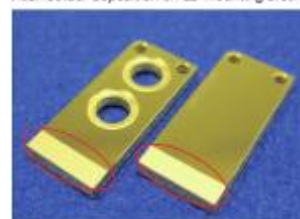


Realized CTE control less than 8ppm/°C by using CuMoCu layer structure with high precision process of Cu surface thickness

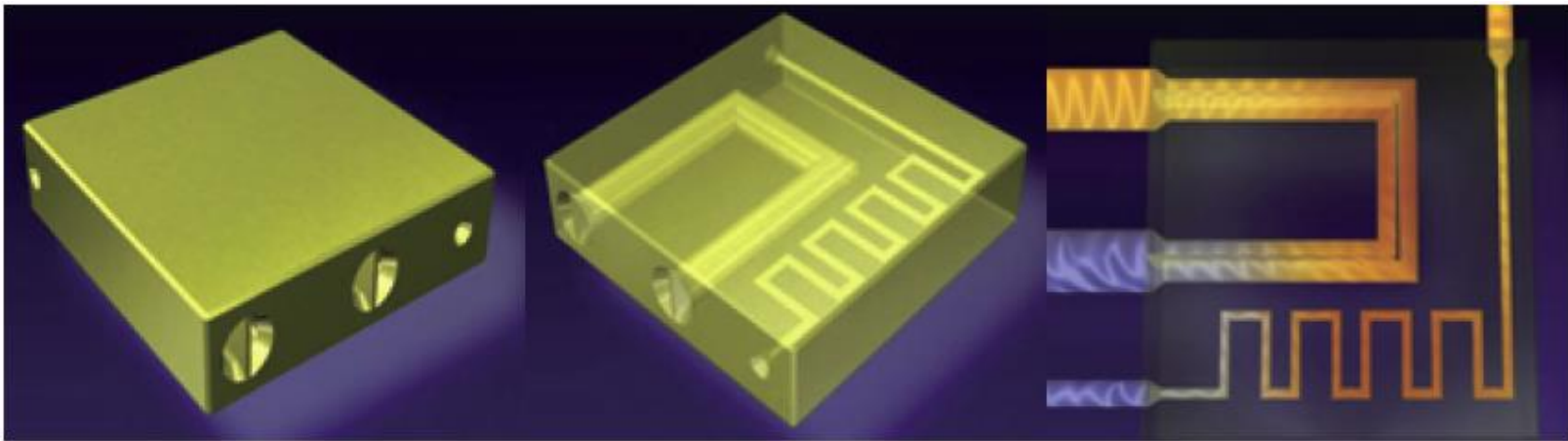
Realize higher power/longer life LD module

- Possible to mount 120W class LD
- Realize CTE 8ppm/°C
 - Possible to mount LD direct on microchannel cooler without submount
- Realize longer life of LD module
 - CTE matching on LD mounting area
 - Au coating on surface of the channel for preventing corrosion
- AuSn solder deposition on LD mounting area
- Joint development with Fraunhofer ILT (Germany)

AuSn solder deposition on LD mounting area



	Features	Remarks
TC	Approx. 0.5°C/W	500ml/min
Flow rate	Approx. 500ml/min	150kPa
Warpage	<1μm	LD mounting area
Size	11.5×26.5×1.55t(mm)	DT process



Realize seamless structure (No bonding layer)

- 3D structure channel
- Inside channel is completely coated by plating
 - Prolong module life by corrosion resistance improvement
- Flexible designing upon requirements
 - Minimum outer dimension : 2.0x2.0x0.6mm
- Solid structure without bonding layer
 - Work under high pressure
 - No liquid / gas leakage

Options

- Add screw tap on joint area
- Diamond turning process
 - Better flatness, sharp edge on device mounting area

Applications

- Heatsinks (water/gas cooling)
- Mixing device
- Analytical device
- Reactor device etc.