Blueberry Semiconductors Pvt. Ltd.

Analog Mixed Signal

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RAM-TECH

Blueberry Semiconductors – *Infinite Possibilities*

Agenda

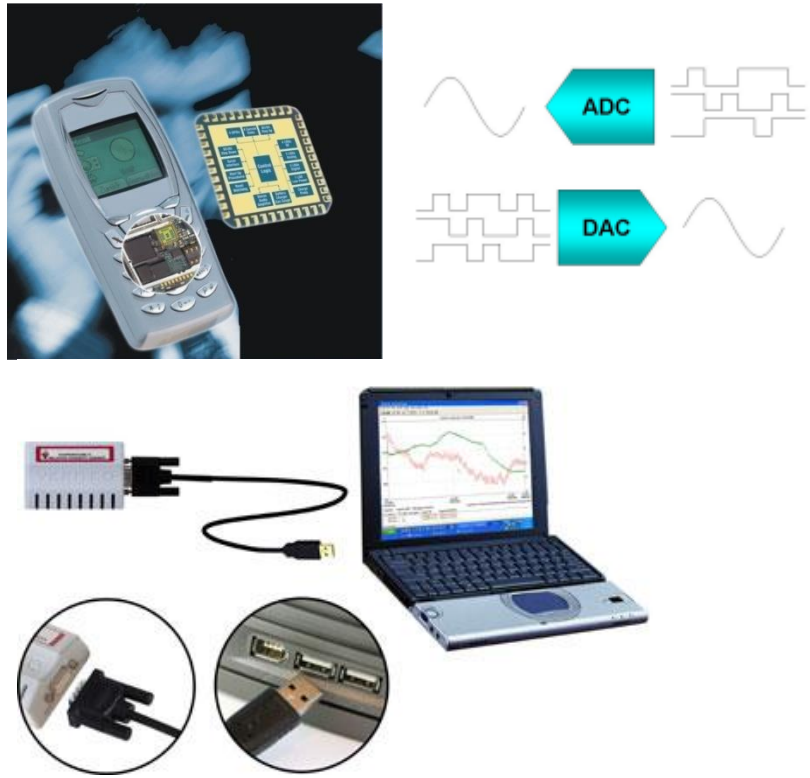
Blueberry Semiconductors Pvt. Ltd.

- Introduction
- Capabilities
- Case Study
- Profile – Offshore Manager

Introduction

Blueberry Semiconductors Pvt. Ltd.

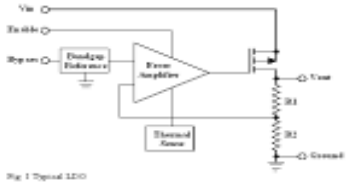
- Analog team lead by highly professional technologists with 50+ years of cumulative industry experience in designing chips for Analog stream of IC design.
- Analog experience, mainly into Power Management
- Also have experience in Signal Processing (converters, Serdes)
- We provide onsite, offsite and offshore technology solutions for all Analog IC design needs.
- In Past we have worked with TSMC, Renesas, NEC, Hitachi-ULSI
- We can provide end to end services comprising front end and back end design(Spec to Silicon).



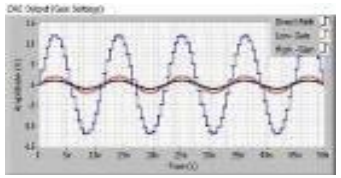
AMS – Capability snapshot

Blueberry Semiconductors Pvt. Ltd.

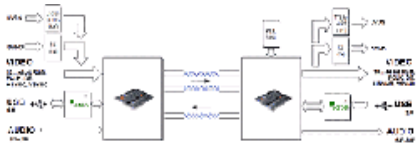
Power Management Circuits



Analog Signal Processing



High-speed Comm Interfaces



- Linear & Switching Regulators
- Reference & Protection Circuits
- Charge Pump
- Temp Sensors

- A/D Converters
- D/A Converters
- Signal Conditioning
- Filters & Amplifiers

- High Speed I/O
- Serial Interface
- Clock Circuits

Analog Modeling & Verification

- Technology Porting : 3 categories

- Circuit Design, Simulation & Analysis
- Block & Full chip Layout,
- IO design & layout

- Modeling & Mixed Signal Verification
- Parasitic Extraction

- Post silicon
- Bench bring-up & testing

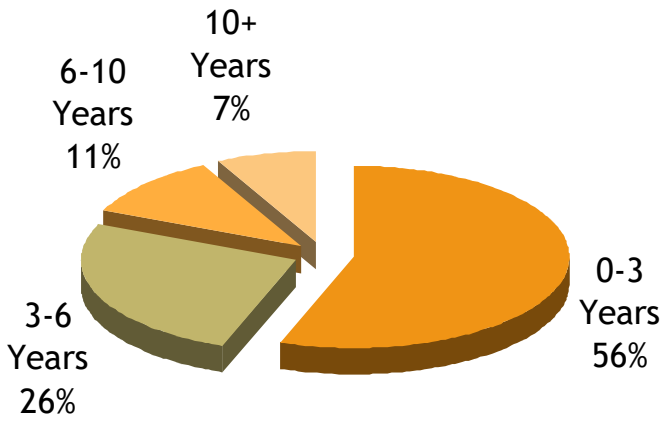
AMS Experience Overview

Blueberry Semiconductors Pvt. Ltd.

Team Size

25+

Design Expertise



Process Experience

Technology*	Variants
45nm to .45u CMOS	• High Speed & Low Power for Analog and Custom Digital blocks • Supply voltages < 1V
0.45u, 0.32µ, 0.15µ	• High voltage CMOS (~15V)
45nm, 65nm, 90nm, 130nm, 150nm	• Generic process • High speed • Low leakage • High voltage variants
0.18µ, 0.15µ, 0.13µ	• RFCMOS process

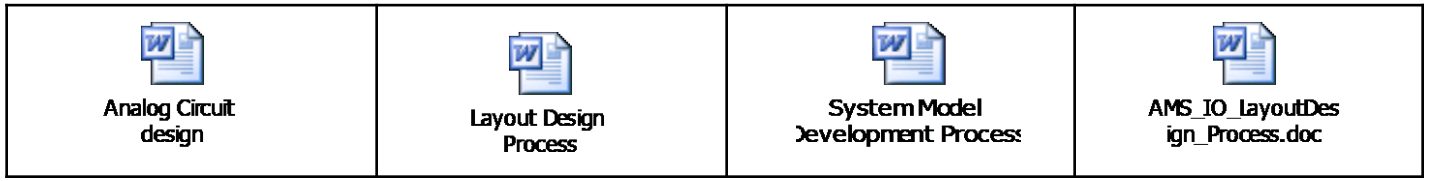
* Includes proprietary process expertise

Analog & Mixed Signal : Quality Process

Blueberry Semiconductors Pvt. Ltd.

- Engineering Process for AMS work flows
  - System Model Development Process "System-Model-Development-Process"
  - Analog Circuit Design Process "Analog Circuit Design"
  - Layout Design Process "Layout-Design-Process"
- Comprehensive Checklists for tracking the various phases of the project
- Strict Peer and Multilevel Reviews
- Detailed and Live Know-how document for all Projects
- Knowledge sharing Repository

Engineering Process documents specific to AMS Practice are attached below :



- Case Study
  - Power Management
  - Converters
  - I/O

Capacitor-less LDO

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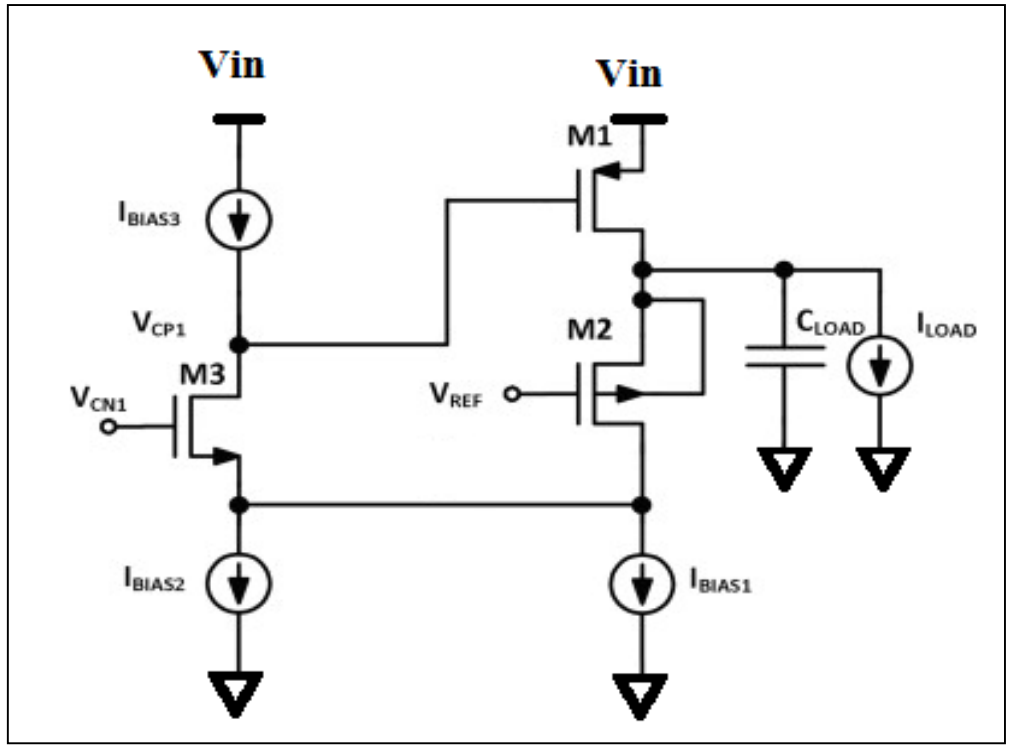
- Capacitor less LDO for low load current Point of Load (POL) application



Foundry : TSMC

Process : 40nm

Load current : 10mA ; Input Voltage : 1.6 to 3.6V

- Features

Low Power SOCs requires many blocks to be turned OFF during power saving modes. Hence there is a need for multiple, Point of Load (POL) Capacitor less LDOs.

The architecture of the LDO will remain same but output voltage and load current remains different for every instance of LDO in the SOC

- Low in area. 0.02mm sq.

DC-DC Converter

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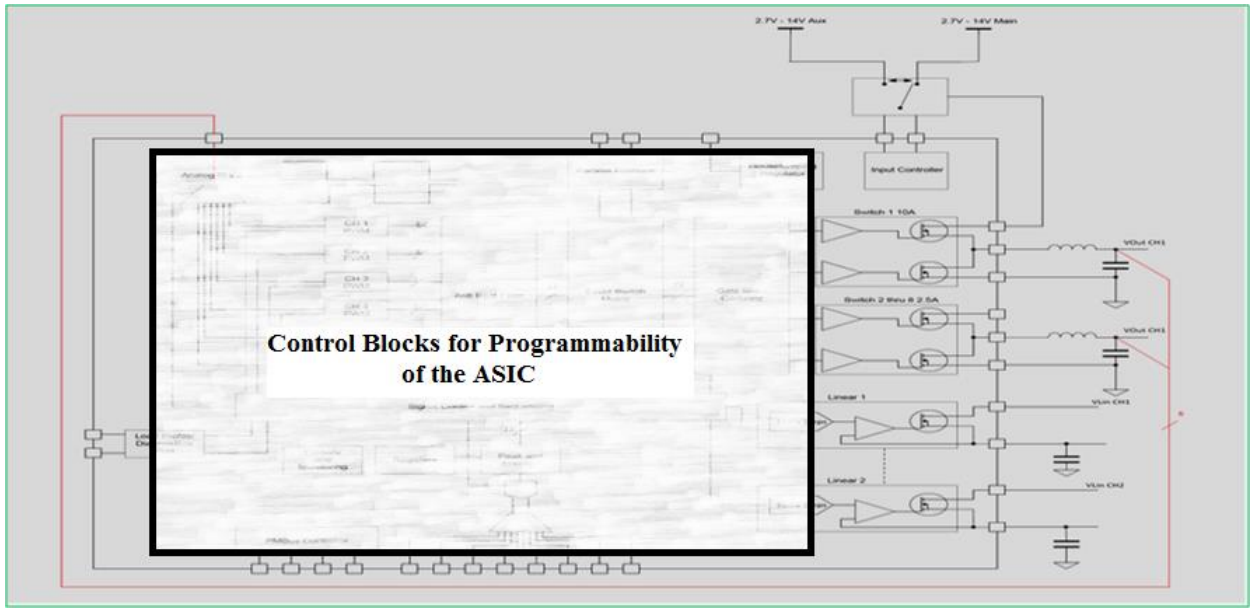
- Programmable Multi-rail DC-DC converter



Foundry : Dongbu

Process : 180nm BCDMOS

Load current: 20A ; Output Voltage: 1V (programmable)

- Features

This innovative single IC addresses applications which need multiple power rails. It comes with a novel idea of programmable output parameters like rail voltage, load current, switching frequency etc which is one of its kind in this industry.

- Highly programmable. Output voltage programmable in steps of 20mV.
- Very high current. Also programmable in by adding 2A switches.

Voltage Doubler

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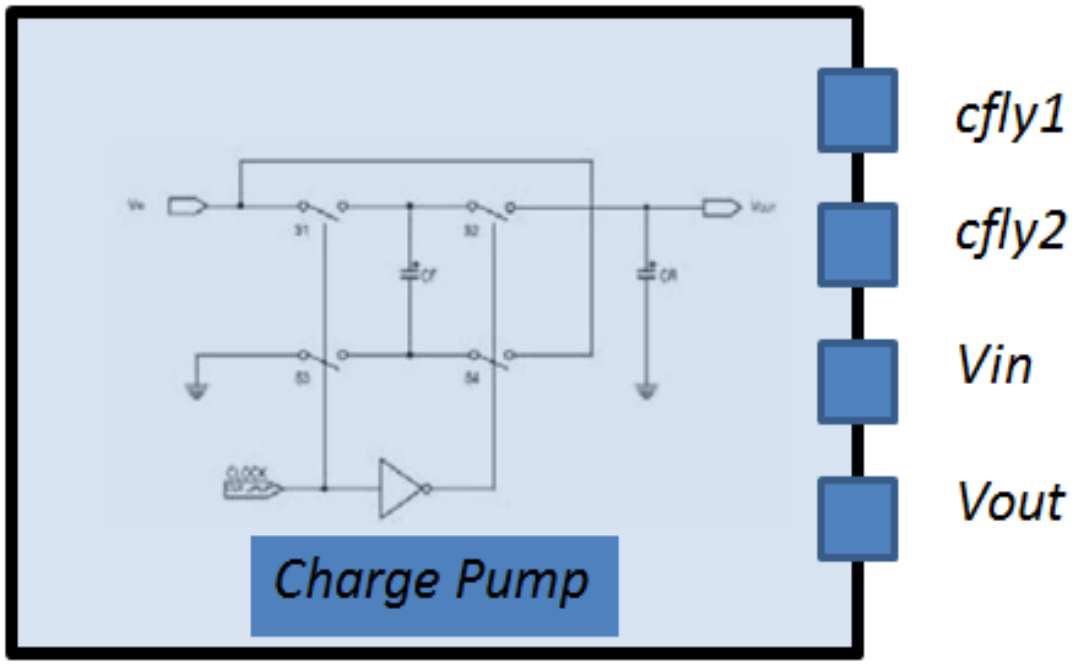
- Charge Pump Voltage Doubler



Foundry : Korean pure play

Process : 180nm BCDMOS

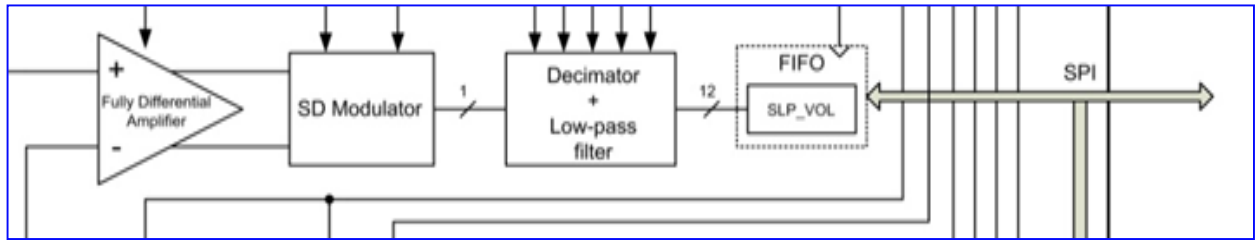
Application: Hand held Gaming console

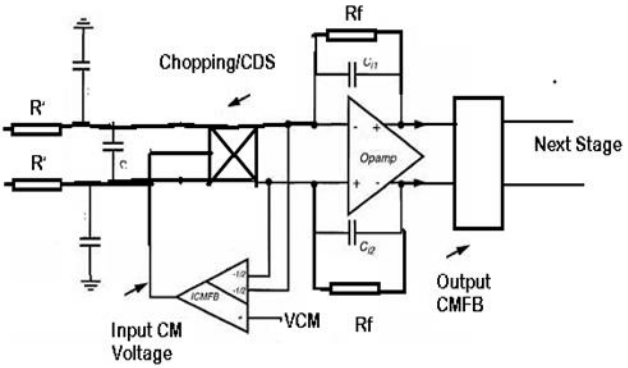
- Features
  - *CP10V:*
    - *Charge pump Doubler*
    - *Input voltage is 5V and Output voltage ~10V*
    - *Soft start circuit has been implemented*
    - *Load current 10mA*

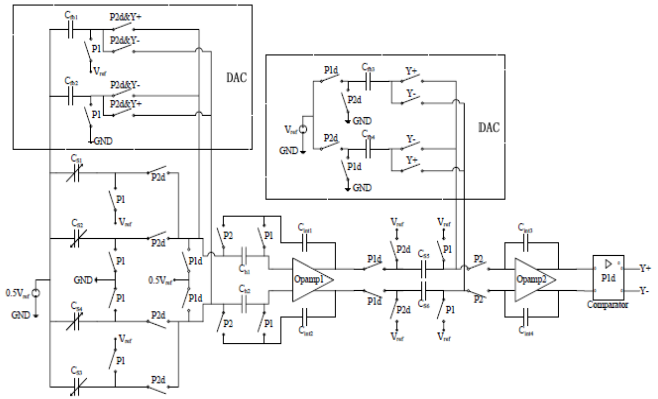
- Output resistance of 2Ω.
- Unregulated charge pump.
- Clock frequency of 500KHz.

ADC

- Sigma Delta ADC







Fab: Custom client process

Tools: Cadence Virtuoso & Matlab

Applications: Automotive for position measurement.

High level specs

- Process Node 65nm
- Signal Bandwidth 2.4kHz
- Oversampling Ratio 1024
- Sampling frequency 5.28MHz
- SNDR (approximate) Min 100dB
- Resolution 12Bits after range conversion
- Temp range -40°C to 140°C

- Challenge:
  - The Area, Power and Speed specifications of this IC, targeted for Consumer application, was challenging

ADC

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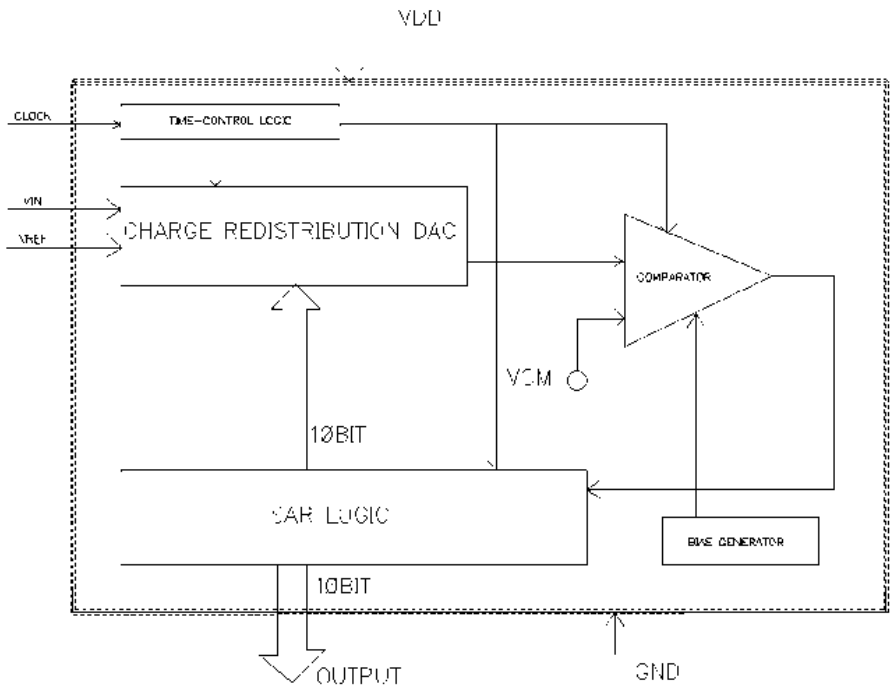
Description

- 10-Bit, 2.0 MSPS SAR ADC



Fab: Custom client process

Tools: Cadence Virtuoso & Matlab

Applications: Automotive for position measurement.

High level specs

- Fully Capacitive, Segmented Charge redistribution DAC
- 3 Stage auto-zeroed Comparator
- DAC Capacitors re-used for I/P Sampling

Scope

- Architecture study & Feasibility analysis using Verilog-A and MATLAB
- Schematic design
- Circuit simulations & characterization
- Layout design and Physical Verification
- Extraction and Post RC Simulations
- Post silicon testing and validation

- Highlight:

I/O Case Studies: Migration

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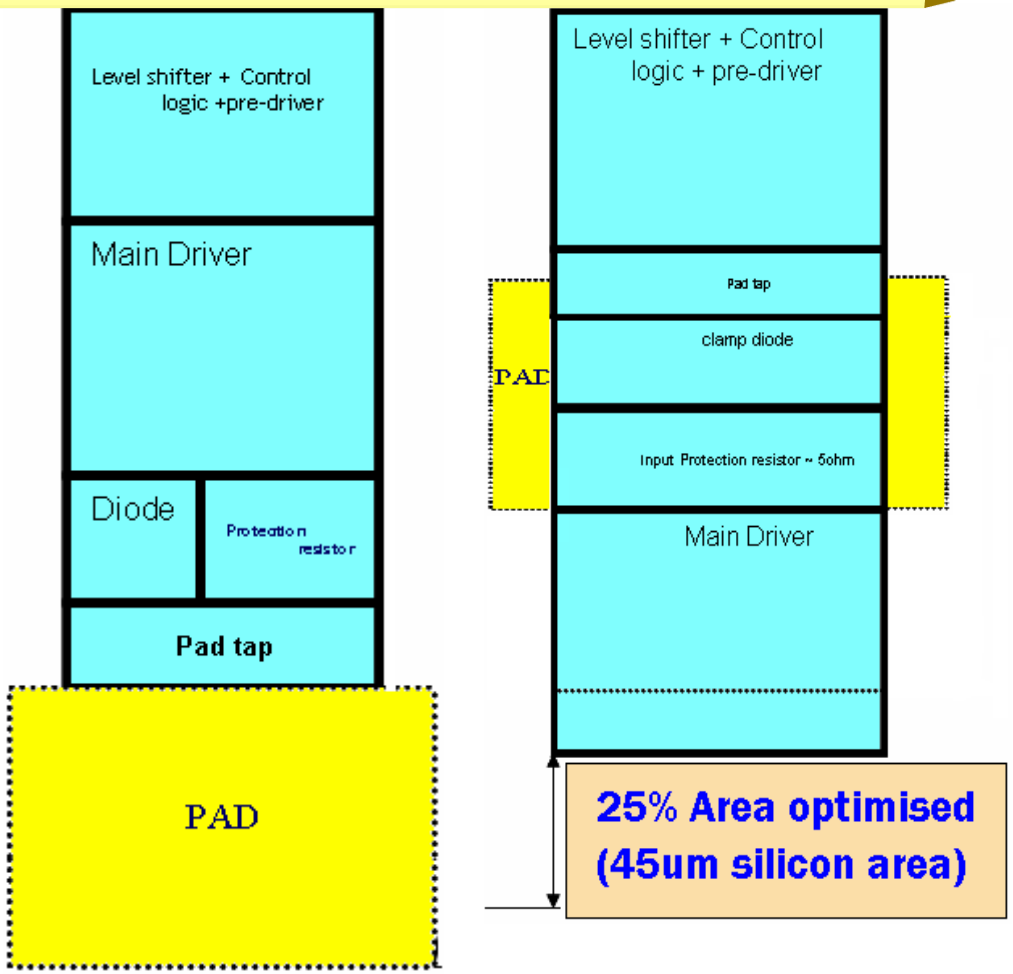
Migration

- Process Migration
  - Have completed numerous projects
  - Have migrated the whole IO libraries from 130nm to 90nm and 65nm
  - Have migrated from ‘G’ process to ‘LP’ process
- Layout migration
  - Have changed the IO cell layouts from ‘non-PAD on IO’ to ‘PAD on IO’ for various process (90nm, 65nm, etc)



I/O Case Studies: std CMOS IO library development

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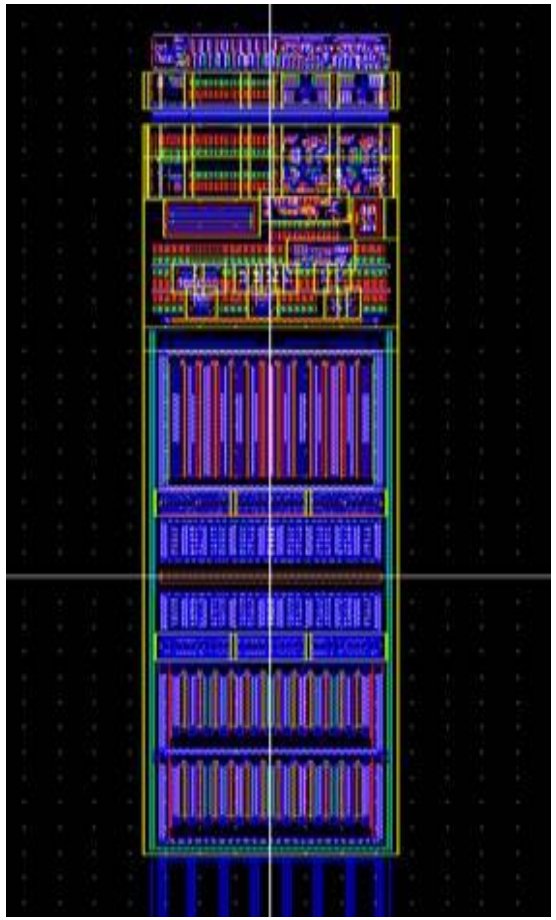
Spec to GDSII : std CMOS IO library

- Development of ~ 150 IO cells
  - Duration: 3 calendar months
  - Team size: 3
  - Process: TSMC 65nm
  - IO cells have different drivability, slew rate control options
  - IO cells include Bi-directional, Input, Output, open drain
  - Our tasks included design, layout (Pad on IO), verification, post-layout validation, combinational verification
  - Simulations include VOH/VOL, VIH/VIL, di/dt, leakage, delay, Tr/Tf, functional
  - Tools used: CADENCE, HSPICE, Calibre, Columbus-AMS, HSIM



Full chip Layout projects

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- *Ultra high current LDO*
  - *Load current : 3A*
  - *Chip size: 2.1 mm X 2.5 mm*
  - *Process: 0.35um BCDMOS*
  - *Foundry : Korean pure play*

- *BLDC Fan Motor Drivers*
  - *Supply Voltages: 15V, 28V & 50V*
  - *Chip size: 2.0 mm X 2.1 mm, 2.8mm X 3 mm*
  - *Process: 0.35um BCDMOS*
  - *Foundry : Proprietary Process*

- *DC DC Buck Converter IC – 2 instances*
  - *Load current : 3A*
  - *Chip size: 5.0 mm X 5.0 mm*
  - *Process: 0.18um BCDMOS*
  - *Foundry : TSMC*

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Thank You

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